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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,411	02/04/2004	Mei Yueh Lu	BHT-3092-414	1911

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EXAMINER
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HESS, DANIEL A

ART UNIT	PAPER NUMBER
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2876

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/770,411

Applicant(s)

LU, MEI YUEH

Examiner

Daniel A. Hess

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 3-10 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 3-6 and 8-10 is/are rejected.  
7) ☒ Claim(s) 7 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

This action is in response to 8/8/2005 response to election / restriction requirement.

### ***Claim Objections***

Claim 7 is objected to under 37 CFR 1.75(c) as being in improper form because it is a multiple dependent claim. This means that it depends from two different independent claims. See MPEP § 608.01(n). Accordingly, the claim 7 has not been further treated on the merits.

Claim 8 is objected to because of the following informalities: The claim is not grammatically proper in that contains no verb. If the words “characterized in that” were removed, the claim would be grammatically proper. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In particular, claim 8 gives three acronyms, MCP, NADN and NOR that are nowhere recited in the specifications and whose meaning is unclear.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-6 and 8-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Kouramanis et al. (US PG PUB 2005/0062858) in view of Dye (US 5,664,162).

Re claim 3: Kouramanis et al. teaches (see especially figure 2 and related discussion in paragraphs [0021] to [0025]) a graphic processor device 250 (incorrectly referred to in the text as 200, which is not visible in figure 2) having a first and second non-volatile memories 204 and 208. In communication with each of these non-volatile memories is a graphics processor 206 that provides digital graphic data processing and computation. There are, as figure 2 shows, two interfaces. Lacking is in the drawing an interface controller, but one skilled in the art knows that one would be present, of some kind. Why? Because a communications line does not directly pour its contents into a memory: such a thing would never work because the memory needs to

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be *addressed*, and handed information bit by bit. [By way of example, we can look at Dye, who teaches a controller: the specification describes (column 5, lines 25-33) an “FPGA” 104 which acts as a controller for the transceivers (i.e. it is a dual interface controller).] After reading to and from the first memory module and second memory module, the result is data to be output at 216b to an external source.

Lacking in Kouramanis et al. is a teaching that the interface is a dual interface.

Dye shows a graphics processor (column 1, lines 10-15) that has dual external data transmission between transceivers 106 and the system bus 102, as is illustrated by the two separate arrows in figure 1 (see column 5, lines 50-55). Dye’s motive for dual interface is clear throughout, faster processing through parallel action.

In view of Dye’s teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the old and well-known dual interface in a graphics processor because through parallel action this can help to achieve faster processing.

Re claims 4 and 5: Making semiconductor components integral is very common. One would only need to open a modern computer processing chip package to discover that there are more than just the transistors of the processor, but also things like on board memory caches of various kinds, all hidden inside the chip packaging.

In view of common integrality of semiconductor components, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the integrations recited in claims 4 and 5 because this would make the processor faster.

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Re claim 6: USB (universal serial bus) standard is a common protocol for communicating with many devices, including a digital camera 212 of Kouramanis et al. USB memory sticks for example have long been employed with digital cameras.

In view of the pervasive use of USB with cameras, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the old and well-known USB for communicating externally in Kouramanis et al. because such a port is already available on most cameras and thus the solution becomes less expensive.

Re claim 8: In general, making semiconductor components integral is very common. One would only need to open a modern computer processing chip package to discover that there are more than just the transistors of the processor, but also things like on board memory caches of various kinds, all hidden inside the chip packaging.

In view of common integrality of semiconductor components, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the integrations recited in claim 8 because this would make the processor faster.

Re claims 9 and 10: See discussion re claim 3, above.

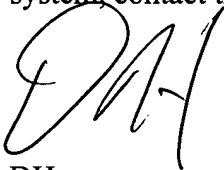
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel A. Hess whose telephone number is (571) 272-2392. The examiner can normally be reached on 8:00 AM - 5:00 PM M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DH  
8/25/05

**DANIEL STCYR  
PRIMARY EXAMINER**

